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Optimisation of Bit Loading in Broadband Power Line Communication Network

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Abstract: *The performance of a Broadband Power Line Communication Network (BPLCN) can be enhanced by using efficient bit loading and power allocation techniques. In this paper, maximization of raw bit rate with optimum allocation of power available for transmission using greedy bit loading is performed in an Orthogonal Frequency Division Multiplexing (OFDM) BPLCN. The performance of bit loading technique is subject to the influence of system parameters such as the load conditions of the power line network, power available for transmission and target error probability. The major focus of this paper is to study the effect of these parameters on the raw bit rates obtained using bit loading. The results simulated using MATLAB are reported and analyzed.*

Keywords: *Bit Loading , Optimisation, Orthogonal Frequency Division Multiplexing, Power Allocation ,Power Line Communication*

I. Introduction

Power line communication technology is used to provide data communication using power lines. The technology operates by impressing a modulated carrier over the wire line system conventionally used for delivering electricity [1]. Interest in this area of communication is increasing owing to the several potential benefits. PLC eliminates the need for installing a dedicated cable for data transmission. The use of existing infrastructure results in cost effectiveness. The technology is highly ubiquitous and therefore can be used to provide communication facilities to rural areas. The technology was initially used only for applications in voice communication (3-3.5 KHz). Today, the technology is suitable for a wide range of applications ranging from home automation to broadband communication [2]. Since power lines were not initially designed for data communication, it acts as a very harsh environment for broadband applications. Therefore, the channel bandwidth used is limited in the range 2-30 MHz.

Orthogonal frequency division multiplexing (OFDM) is a suitable technique for implementing PLC since it provides many significant advantages such as interference resistance and flexibility over other techniques [3]. Moreover, bit loading and power allocation techniques further improve the performance of such systems by efficient utilization of available power to improve bit rates.

In [4], a simple bit loading technique for OFDM systems is discussed. Bit loading in time varying power line channels is discussed in [5], [6]. In this paper, bit loading is conducted in a more generalized and flexible BPLCN model and the effect of parameters such as different load conditions, available power and target error probability on the results of bit loading is analyzed.

The remaining sections of the paper are organized as follows. Section II describes the model of the broadband power line communication network (BPLCN) chosen for performing the analysis. Section III explains the bit loading technique. Section IV analyses the effect of system parameters on bit loading. Finally, section V concludes the paper.

II. Communication System Model

The power line communication system model chosen for this work is shown in Fig.1. It is a generalized system model with a central service panel (SP) connected to distribution boxes (DB) and several outlets For an in-home communication system, the different distribution boxes can be considered as last mile connections and each outlet can be considered as an end device.

In the generated topology, there are four distribution boxes, which are connected directly to the service panel. Each distribution box is connected to the service panel at different lengths. The different lengths in meters are as shown in Fig. 1.

The distribution boxes are in turn connected to several outlets. The distribution boxes and outlets are connected using star topology. For connection between a distribution box and the corresponding outlets, lengths between a minimum length of 3m and a maximum length of 10m is chosen. Each outlet is considered as terminating impedance for the system.

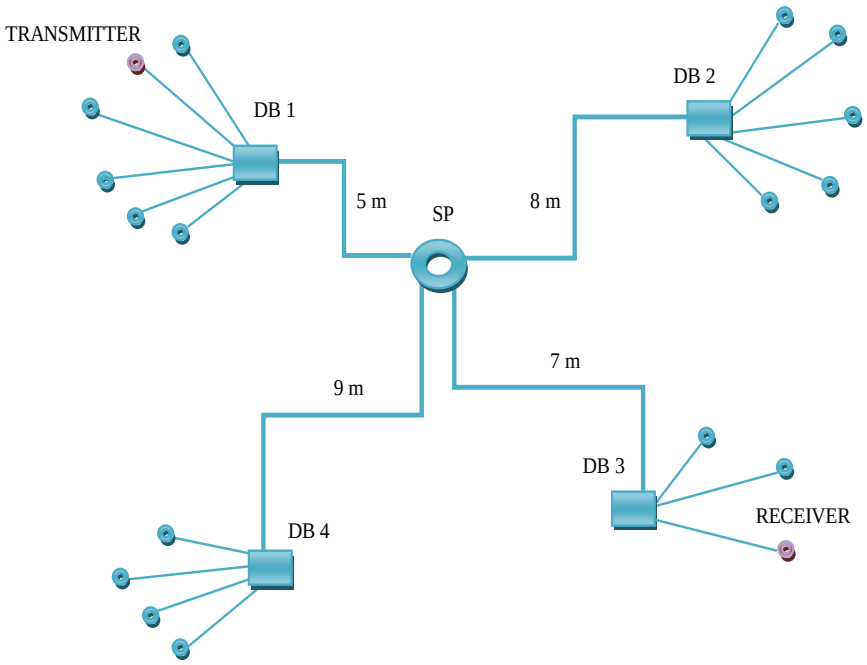

Figure 1. Communication system model.

Communication is made from the transmitter outlet to the receiver outlet. In the selected BPLCN, second outlet of first derivation box is chosen as the transmitter and the third outlet of third derivation box is chosen as the receiver. The model is based on [7], [8] and [9]. Simulator for the model is available at [10]. The frequency response for the above described channel model is simulated in the frequency range of 2-30 MHz and is shown in Fig.2. The magnitude response of the channel varies with the variation in frequency.

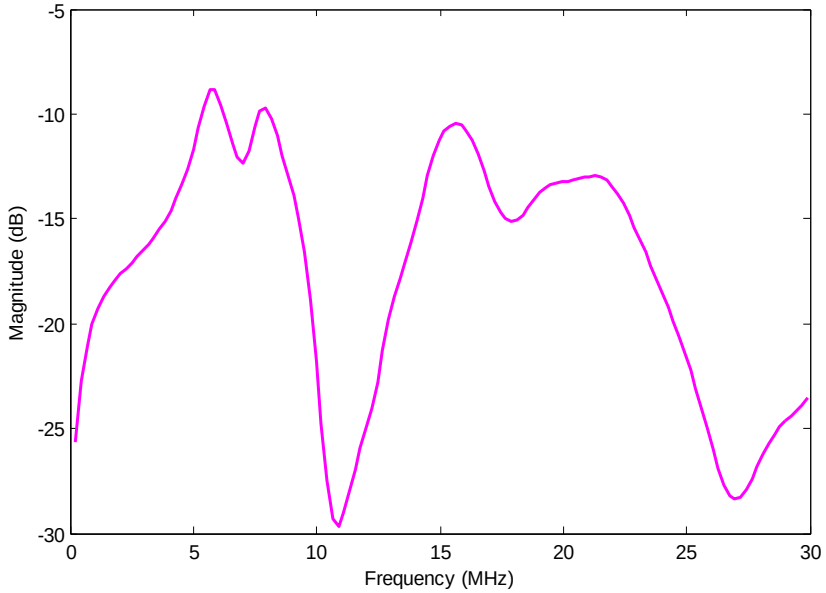

Figure 2. Channel Frequency Response

III. Bit Loading

In this paper, a greedy type optimization algorithm is used for bit loading. Such algorithms work better than conventional water filling techniques in terms of optimisation. The technique tries to obtain an optimum solution which maximizes the total number of bits transmitted and is subject to the constraint that the total power across sub channels does not exceed the maximum available power for transmission as given in equation (1) and (2).

maximise : $$N_b = \sum_{k=1}^{N} B_k \quad (1)$$

subject to constraint : $$\sum_{k=1}^{N} P_k < P_{\max} \quad (2)$$

where N , B_k , N_b , P_k , $P_{\max}$ represents number of sub channels, number of bits in each sub channel, total number of bits transmitted, power in each sub channel and maximum available power for transmission respectively. For the purpose of this work, the entire channel bandwidth of 2-30 MHz is considered for the power line communication system. The spectrum is then divided into a number of 128 sub channels across which bit loading is conducted. In this work, bit loading is done only across frequency. The bit loading process continues until the power across all sub channels stays within the limit of maximum available power for transmission. The algorithm is designed for a given symbol error probability using the relation for QAM symbols as given in [6].

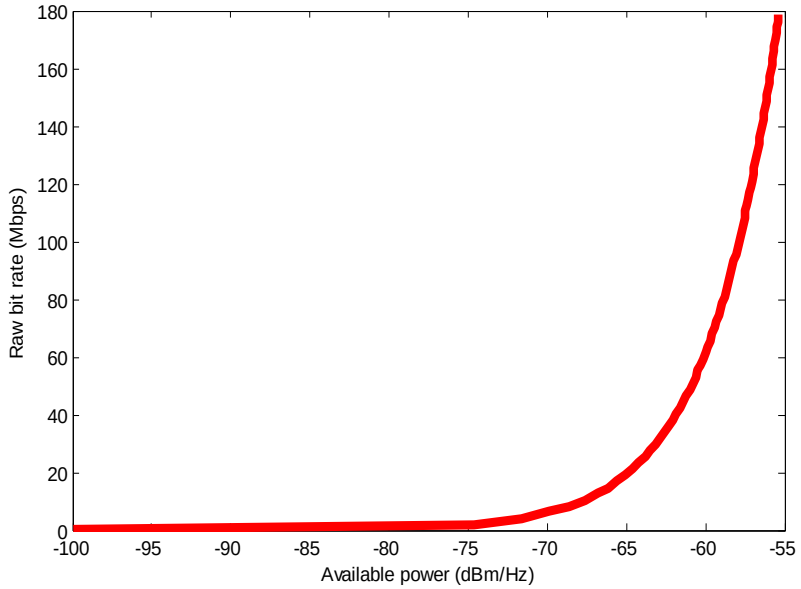

Figure 3. Result of bit loading

The result of bit loading for the chosen system is shown in Fig. 3. The result is obtained for a target symbol error probability of 10^{-5} and a noise power spectral density of -110 dBm/Hz considering additive white Gaussian (AWGN) noise. The raw bit rates achieved at different levels of available power is reported. Therefore, the result also shows the influence of variation in power available for transmission on the result of bit loading. The results are simulated for available power values ranging from -100 dBm/Hz to -55 dBm/Hz. It can be observed from the results that transmission does not take place at lower power levels . Transmission takes place only when the power requirement of the system is met with the power available for transmission. For the selected system, transmission starts only when the available power is around -75 dBm/Hz which shows that the minimum power requirement of the system lies in that range. At higher power levels, additional power available is used to further increase raw bit rates. At high power levels, considerably good amount of bit rates are obtained. Maximum raw bit rates of around 180 Mbps is obtained for a maximum available power of -55 dBm/Hz using greedy bit loading technique.

IV. Effect Of System Parameters

The performance of bit loading technique is subject to the influence of certain system parameters. Major design parameters include the different load conditions for the chosen BPLCN system, power available for transmission and the target error probability. Results of the technique vary for different values of these parameters. Influence of power available for transmission has already been discussed in the previous section. The effect of the other parameters on the results of bit loading are analyzed and reported in the following subsections.

1. Variation in Load Condition

For the selected BPLCN system model, different numbers of outlets are connected to different distribution boxes. Since each outlet is a terminating impedance for the system, change in total number of outlets change the load condition of the system. By varying the number of outlets in each derivation box and thereby the load condition, the corresponding effect on obtained bit rates can be studied. Different cases considered for analyzing the variation of number of outlets on bit loading is shown in Table 1.

Table 1. Cases Selected

Case	Number of outlets			
	Derivation box 1	Derivation box 2	Derivation box 3	Derivation box 4
1	6	5	3	4
2	7	6	4	5
3	8	7	5	6
4	9	8	6	7

Case 1 corresponds to the channel model chosen initially. In each of the other cases number of outlets in each derivation box is increased by a factor of one from the previous case thereby increasing the total number of outlets by a factor of four each time.The result of the effect of the variation in number of outlets at different levels of available power is shown in Fig. 4.

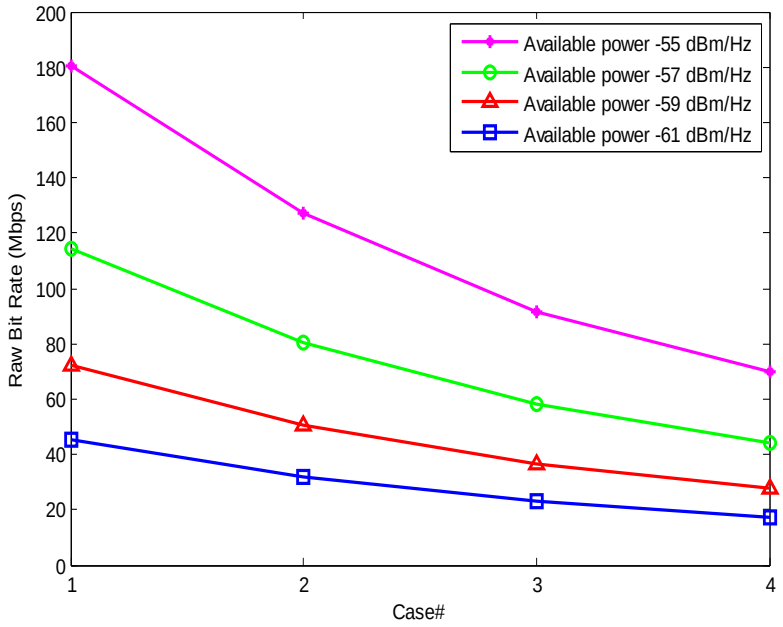

Figure 4. Effect of variation in load condition

Results show that raw bit rates tend to decrease with the increase in the total number of outlets. Effective impedance and the effective attenuation of the system increase with the increase in number of outlets thereby decreasing the raw bit rates. Results are shown for different values of available power ranging from -61 dBm/Hz to -55 dBm/Hz. It has been observed that the obtained raw bit rate decreases with the decrease in the available power.

2. Variation in Target Error Probability

The bit loading algorithm works for a specific given target error probability. Raw bit rates obtained change for different values of target error probability. This change happens due to the change in power requirement of the system for different values of target error probability. Results of the effect of variation in target error probability for the four cases chosen earlier are as shown in Fig. 5.

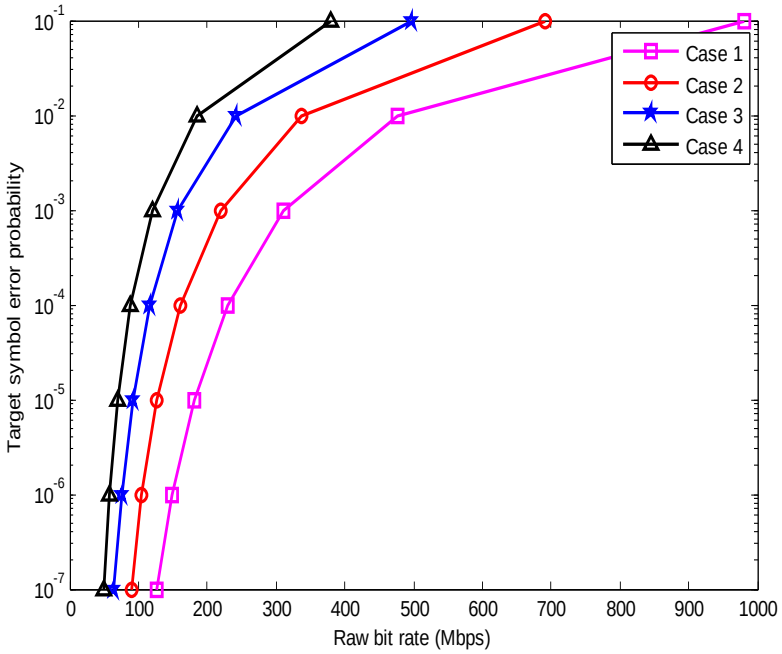

Figure 5. Effect of variation in target error probability

Raw bit rate is simply the total physical number of bits which could be transmitted per second through the channel. It is not the number of bits which reaches the receiver without error as in the case of capacity. Therefore, increase in raw bit rates always come with a cost of increased error probability. The results show the different values of target error probability and the corresponding raw bit rates achieved. Design of the communication system must be performed such that the probability of error is low at the same time providing considerably good amount of raw bit rate for a given load condition for the chosen system.

V. Conclusion

In this work, optimum bit loading for BPLCN was conducted and the effect of system parameters on bit loading was analyzed. Maximum raw bit rates of around 180 Mbps was obtained using greedy bit loading. Results show that obtained raw bit rates are subject to large influence of parameters such as available power, different load conditions and target error probability. Transmission takes place only if the available power meets system power requirements and raw bit rates obtained increase with increase in power available for transmission. Change in load conditions influence bit loading in such a way that increase in effective impedance decrease raw bit rate. Increase in raw bit rates come at the cost of increase in probability of error. The challenge for future work in this area is to make the raw bit rates independent of the influence of these parameters.

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